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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,296	12/15/2003	Yuji Yamasaki	60188-733	4712

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EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/734,296	YAMASAKI ET AL.	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/15/04, 12/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the ile.

Information Disclosure Statement (IDS) filed on 4/15/04 and 12/15/03 were considered.

2. Claims 1-32 are presented for examination.

Claim Rejections - 35 USC э 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimoto et al, Pat. No. 6781915.

With regard to claim 1, Arimoto discloses memory device comprising: a word line (fig. 4, WL0); a first bit line (fig. 4, BLL) intersecting with the word line; a second bit line (fig. 4, ZBLL) forming a bit line pair with the first bit line; a memory cell including an access transistor (fig. 1, MTR) of an MISFET in which a gate electrode (fig. 5, 13) is connected to the word line (fig. 4, WL0) and a first doped layer (fig. 5, 12a) is connected to the first bit line, and a cell capacitor (fig. 5, 15 (CP)) connected to a second doped

layer of the access transistor (fig. 5, 12b), being capable of storing electric charge, and located at the intersection between the word line and the first bit line (col. 6, line 64-col. 7, line 7); and a sense amplifier (fig. 4, SA) for amplifying a potential difference between the first bit line the second bit line during a read-out operation (col. 7, line 59-65), wherein a positive power supply voltage is applied to the first bit line in a high level state and a ground voltage is applied to the first bit line in a low level state (col. 3, line 50-53) (col. 13, line 4-13), wherein the access transistor is a depletion type p-channel MISFET (fig. 1. MTR) (col. 6, line 54-56) (col. 7, line 3-7) (also with regard to claim 3); and wherein the ground voltage is applied to a gate electrode of the access transistor through the word line when the memorycell is in an activated state (col. 12, line 56-59) (also with regard to claim 5).

With regard to claim 2, Arimoto discloses wherein an increased potential higher than the positive power supply voltage is applied to the gate electrode of the access transistor in a non-activated state (col. 13, line 23-25).

With regard to claim 4, Arimoto discloses wherein the cell capacitor is a planar type MISFET (col. 10, line 65-68) (also with regard to claim 19).

With regard to claim 6, Arimoto discloses wherein the access transistor and the cell capacitor share a substrate or an n-type well to which the positive power supply voltage is applied (fig. 5, sharing substrate N).

With regard to claim 7 and 24, Arimoto discloses wherein the sense amplifier includes: an amplifier circuit which includes a pair of p-channel MISFETs (fig. 18, 63-64) and amplifies a potential difference between the pair of bit lines; and a p-channel

drive MIS transistor (fig. 18, 60) which controls (by the sense enabling signal SOP) driving of the amplifier circuit and has a lower threshold voltage than that of the pair of p-channel MISFETs (col. 2, line 39-64) (also with regard to claim 8 and 25).

With regard to claim 9, Arimoto discloses a precharging/equalizing circuit including a bit line equalizing transistor of a depletion type p-channel MISFET for short-circuit between the first bit line and the second bit line during a period in which the memory cell is in a non-activated state (col. 12, line 35-55); a bit line precharing transistor of depletion type p-channel MISFET for applying a constant voltage to the bit line pair during a period in which the memory cell is in a non-activated state (col. 12, line 22-36) (also with regard to claim 10, 26, 27)

With regard to claim 11, Arimoto discloses wherein the access transistor, the bit line equalizing transistor, the bit line precharging transistor and the pair of p-channel MISFETs in the sense amplifier are formed in a common process step (col. 7, line 1-17) (also with regard to claim 28).

With regard to claim 12, Arimoto discloses memory device comprising: a word line (fig. 4, WL0); a first bit line (fig. 4, BLL) intersecting with the word line; a second bit line (fig. 4, ZBLL) forming a bit line pair with the first bit line; a memory cell including an access transistor (fig. 1, MTR) of an MISFET in which a gate electrode (fig. 5, 13) is connected to the word line (fig. 4, WL0) and a first doped layer (fig. 5, 12a) is connected to the first bit line, and a cell capacitor (fig. 5, 15 (CP)) connected to a second doped layer of the access transistor (fig. 5, 12b), being capable of storing electric charge, and located at the intersection between the word line and the first bit line (col. 6, line 64-col.

7, line 7); and a sense amplifier (fig. 4, SA) for amplifying a potential difference between the first bit line the second bit line during a read-out operation (col. 7, line 59-65), wherein a positive power supply voltage is applied to the first bit line in a high level state and a ground voltage is applied to the first bit line in a low level state (col. 3, line 50-53) (col. 13, line 4-13), wherein the access transistor is a depletion type n-channel MISFET (fig. 12. MTR) (col. 6, line 54-56) (col. 7, line 3-7) (also with regard to claim 14, and 31); and wherein the positive voltage is applied to a gate electrode of the access transistor through the word line when the memory cell is in an activated state (col. 3, line 50-52) (fig. 12, Vp=Vccs +&) (col. 15, line 12-15) (also with regard to claim 30).

With regard to claim 13, Arimoto discloses wherein a negative increased potential lower than the ground voltage is applied to the gate electrode of the access transistor in a non-activated state (col. 3, line 53-57).

With regard to claim 15 and 32, Arimoto discloses wherein the sense amplifier includes: an amplifier circuit which includes a pair of n-channel MISFETs (fig. 18, 65-66) and amplifies a potential difference between the pair of bit lines; and a n-channel drive MIS transistor (fig. 18, 62) which controls (by the sense enabling signal SON) driving of the amplifier circuit and has a lower threshold voltage than that of the pair of n-channel MISFETs (col. 2, line 39-64).

With regard to claim 16 and 29, Arimoto discloses memory device comprising: a logic circuit (fig. 1, logic 2) which includes a p-channel MISFET and is integrated on a substrate; and a dynamic memory device (fig. 1, DRAM CORE 3) provided on the substrate on which the logic circuit is provided and including a word line (fig. 4, WL0); a

first bit line (fig. 4, BLL) intersecting with the word line; a second bit line (fig. 4, ZBLL) forming a bit line pair with the first bit line; a memory cell including an access transistor (fig. 1, MTR) of a p-channel MISFET in which a gate electrode (fig. 5, 13) is connected to the word line (fig. 4, WL0) and a first doped layer (fig. 5, 12a) is connected to the first bit line, and a cell capacitor (fig. 5, 15 (CP)) connected to a second doped layer of the access transistor (fig. 5, 12b), being capable of storing electric charge, and located at the intersection between the word line and the first bit line (col. 6, line 64-col. 7, line 7); and a sense amplifier (fig. 4, SA) for amplifying a potential difference between the first bit line the second bit line during a read-out operation (col. 7, line 59-65), wherein the threshold voltage of the access transistor is set to be higher than that of the p-channel MISFET provided in the logic circuit (col. 6, line 54-59).

With regard to claim 17, Arimoto discloses wherein the access transistor is a depletion type MISFET (col. 7, line 1-7) (col. 6, line 54-56) (also with regard to claim 18); wherein the ground voltage is applied to a gate electrode of the access transistor through the word line when the memory cell is in an activated state (col. 8, line 24-26) (also with regard to claim 20).

With regard to claim 21, Arimoto discloses wherein the access transistor includes a gate insulation film having a greater thickness than the thickness of a gate insulation film of the p-channel MISFET in the logic circuit (fig. 9).

With regard to claim 22, Arimoto discloses wherein the thickness of the gate insulation film of the access transistor equal to the thickness than the thickness of a gate insulation film of the cell capacitor (col. 4, line 4-7).

With regard to claim 23, Arimoto discloses wherein the access transistor and the cell capacitor share a substrate or an n-type well to which the positive power supply voltage is applied (fig. 8, same substrate 11), and wherein the positive power supply voltage is applied to the first bit line in a high level state and the ground voltage is applied to the first bit line in a low level state (col. 3, line 50-53) (col. 13, line 4-13).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Yamauchi et al (6088286), Tsuruda et al (5872737) and Yamasaki (6631092) disclose a memory device.

5. When responding to the office action, Applicants= are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

6. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to

the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov Should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

July 2005

CONNIE C. YOHA
PRIMARY EXAMINER